MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 1, 2015/2016

EEE3106 – PROCESSING AND FABRICATION TECHNOLOGY

(EE)

13 OCTOBER 2015
02:30 p.m. - 04:30 p.m.
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of 6 pages with 3 Questions only.
2. Attempt **ALL THREE** questions. The distribution of the marks for each question is given.
3. Please print all your answers in the Answer Booklet provided.
4. Please refer to APPENDIX at page 6 for the error function table.

QUESTION 1

(a) The Czochralski (CZ) process is the most important production technique for high quality silicon (Si) single crystals. Answer the following:

(i) With the aid of a suitable diagram, explain how the CZ technique is used to obtain a doped single crystal Si boule.

[3+6 marks]

(ii) With the aid of a suitable equation, discuss the dopant distributions along the Si boule grown using CZ technique when the segregation coefficient of the dopant is *larger than 1* and *smaller than 1* respectively.

[1+4 marks]

(b) Flat grinding is a silicon (Si) wafering process where one or more flats are grinded along the entire length of the Si boule. Answer the following:

(i) Give the **TWO(2)** functions of the flats.

[2 marks]

(ii) Sketch and label the {111} and {100} *p*-type Si wafer respectively.

[4 marks]

QUESTION 2

(a) Photolithography can be classified in terms of the types of exposure methods used for imaging a mask pattern onto the resist; which are *contact*, *proximity*, and *projection*. Discuss briefly the working principles and highlight the major strength of these three types of exposure methods respectively.

[6+3 marks]

(b) Chemical vapor deposition (CVD) is a process whereby a thin solid film is deposited from vapor-phase precursors by chemical reactions occurring on or in the vicinity of a normally heated substrate surface. Answer the following:

(i) Differentiate *surface-controlled growth* and *mass-controlled growth* in a CVD process.

[6 marks]

(ii) Which type of CVD reactor will be your choice, atmospheric pressure (APCVD) or low pressure (LPCVD), if both film uniformity and step coverage are among your considerations? Justify your selection.

[1+2 marks]

Continued...

(c) In semiconductor integrated circuits fabrication, diffusion is a technique to introduce dopant atoms into the silicon lattice. The diffusion process is usually done in two-steps sequence: *predeposition* and *drive-in*. Answer the following:

(i) Using suitable explanations, distinguish the predeposition and the drive-in diffusions.

[4 marks]

(ii) A predeposition diffusion process is carried out by introducing phosphorus (P) atoms into a *p*-type silicon (Si) wafer having background concentration of 10^{18} atoms·cm^{-3} at 800 °C for 30 minutes. Given that the diffusion coefficient of phosphorus at 800 °C in silicon is 2.6×10^{-17} cm^2·s^{-1} and its solid solubility limit is 2.79×10^{20} atoms·cm^{-3}. Determine the junction depth.

[4 marks]

(d) Aluminum (Al) is a popular metal used to interconnect integrated circuits because this material does not diffuse into silicon dioxide substrate and it adheres well to both silicon and silicon dioxide.

(i) Discuss the possible root cause contributing to the mean-time-to-failure in an aluminium interconnect which has been operated at relatively high current densities.

[4 marks]

(ii) Suggest **ONE(1)** solution to solve this failure.

[1 mark]

(e) Self-aligned silicidation (salicide) process is used to form silicides simultaneously at source/drain and gate regions without the need of an additional lithography step. Explain the fabrication processes to obtain salicide.

[4 marks]

(f) **Fig. Q2(f)** shows the cross-section of a gate injection transistor. This transistor is composed of a p-AlGaN/i-AlGaN/i-GaN heterostructure grown on a Si substrate with buffer layer consisting of the GaN/AlN multilayers ontop of the AlGaN/AlN initial layer, and Ti/Al source/drain contacts and Pd gate metal. *(AlGaN: aluminum gallium nitride, GaN: gallium nitride, AlN: aluminum nitride, Si: silicon, Ti: titanium, Al: aluminum, Pd: palladium, i: insulating)* Answer the following:

(i) Using *schematic illustrations*, create the necessary processing steps to completely fabricate the transistor given in **Fig. Q2(f)** beginning from a Si substrate.

[9 marks]

(ii) Sketch the **THREE(3)** patterned masks which are required throughout the fabrication processes of the transistor assuming that positive photoresist (+PR) is used during the lithography process.

[6 marks]

Continued...

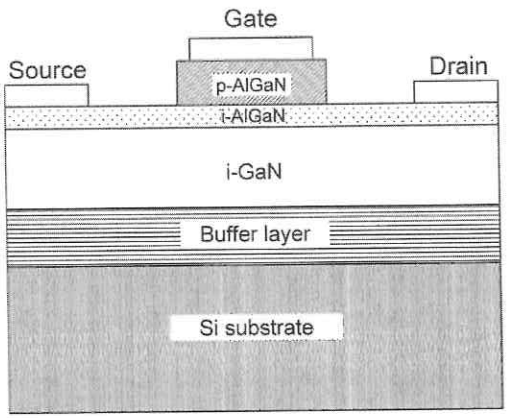

Fig. Q2(f)

QUESTION 3

(a) Wafer test is performed after the circuitry has been fabricated onto the wafer, whereby each individual die is checked for its parameters, functionality, and performance, before being separated from the wafer. Answer the following:

(i) What are the main purposes of the two types of electrical tests, *parametric* and *functional* tests, respectively?

[3 marks]

(ii) Explain briefly how the electrical tests are carried out on the chips?

[3 marks]

(b) There are two common processes to attach die to the pad or cavity of the package's support structure, namely *epoxy adhesive* and *eutectic die attach*. Using suitable explanations, distinguish these two die attachment processes.

[8 marks]

(c) In the world of high-speed/high-performance package design, the primary packaging solution is flip-chip packaging technology. It offers a variety of benefits compared to traditional wire-bond packaging. Using suitable explanations, evaluate the flip-chip technology in the context of *reliability*, *functionality*, and *cost*, in comparison to wire-bond packaging.

[6 marks]

Continued...

(d) A 300 mm silicon (Si) wafer used to make 5×5 mm^2 dies has defect density of 2 defects·cm^{-2} with the same defect density everywhere. The cost to complete the wafer processes is RM1500, the cost for packaging and testing is RM2.70 per die, and the market price for a packaged die is RM3.50. Answer the following:

(i) Calculate the wafer yield.

[2 marks]

(ii) What is the total manufacturing cost for a packaged die?

[4 marks]

(iii) Determine the wafer yield needed for the manufacturing cost to drop below the market price.

[2 marks]

(iv) If the costs of packaging and testing drops to RM1.50 per die upon process optimization, what must be the wafer yield for the manufacturing cost to drop below the market price,?

[2 marks]

Continued...

APPENDIX

Values of the error function $\operatorname{erf}(t) = \frac{2}{\sqrt{\pi}} \int_0^t e^{-a^2} da$

t	0	1	2	3	4	5	6	7	8	9
0.0	0.000	0.0113	0.0226	0.0338	0.0451	0.0564	0.0676	0.0789	0.0901	0.1013
0.1	0.1125	0.1236	0.1348	0.1459	0.1569	0.1680	0.1790	0.1900	0.2009	0.2118
0.2	0.2227	0.2335	0.2443	0.2550	0.2657	0.2763	0.2869	0.2974	0.3079	0.3183
0.3	0.3286	0.3389	0.3494	0.3593	0.3694	0.3794	0.3893	0.3992	0.4090	0.4187
0.4	0.4284	0.4380	0.4475	0.4569	0.4662	0.4755	0.4847	0.4937	0.5027	0.5117
0.5	0.5205	0.5292	0.5379	0.5465	0.5549	0.5633	0.5716	0.5798	0.5879	0.5959
0.6	0.6039	0.6117	0.6194	0.6270	0.6346	0.6420	0.6494	0.6566	0.6638	0.6708
0.7	0.6778	0.6847	0.6914	0.6981	0.7047	0.7112	0.7175	0.7238	0.7300	0.7361
0.8	0.7421	0.7480	0.7538	0.7595	0.7651	0.7707	0.7761	0.7814	0.7867	0.7918
0.9	0.7969	0.8019	0.8068	0.8116	0.8163	0.8209	0.8254	0.8299	0.8342	0.8385
1.0	0.8472	0.8468	0.8508	0.8548	0.8586	0.8624	0.8661	0.8698	0.8733	0.8768
1.1	0.8802	0.8835	0.8868	0.8900	0.8931	0.8961	0.8991	0.9020	0.9048	0.9076
1.2	0.9103	0.9130	0.9155	0.9181	0.9205	0.9229	0.9252	0.9275	0.9297	0.9319
1.3	0.9340	0.9361	0.9381	0.9400	0.9419	0.9438	0.9456	0.9473	0.9490	0.9507
1.4	0.9523	0.9539	0.9554	0.9569	0.9583	0.9597	0.9611	0.9624	0.9637	0.9649
1.5	0.9661	0.9673	0.9684	0.9695	0.9706	0.9716	0.9726	0.9736	0.9746	0.9755
1.6	0.9764	0.9772	0.9780	0.9789	0.9796	0.9804	0.9811	0.9818	0.9825	0.9832
1.7	0.9838	0.9844	0.9850	0.9856	0.9861	0.9867	0.9872	0.9877	0.9882	0.9886
1.8	0.9891	0.9895	0.9899	0.9904	0.9907	0.9911	0.9915	0.9918	0.9922	0.9925
1.9	.99279	.99309	.99338	.99366	.99392	.99418	.99443	.99466	.99489	.99511
2.0	.99532	.99552	.99572	.99591	.99609	.99626	.99642	.99658	.99673	.99688
2.1	.99702	.99715	.99728	.99741	.99753	.99764	.99775	.99785	.99795	.99805
2.2	.99814	.99822	.99831	.99839	.99846	.99854	.99861	.99867	.99874	.99880
2.3	.99886	.99891	.99897	.99902	.99906	.99911	.99915	.99920	.99924	.99928
2.4	.99931	.99935	.99938	.99941	.99944	.99947	.99950	.99952	.99955	.99957
2.5	.99959	.99961	.99963	.99965	.99967	.99969	.99971	.99972	.99974	.99975
2.6	.99976	.99978	.99979	.99980	.99981	.99982	.99983	.99984	.99985	.99986
2.7	.99987	.99987	.99988	.99989	.99989	.99990	.99991	.99991	.99992	.99992
2.8	.99992	.99993	.99993	.99994	.99994	.99994	.99995	.99995	.99995	.99996
2.9	.99996	.99996	.99996	.99997	.99997	.99997	.99997	.99997	.99997	.99998
3.0	.99998	.99998	.99998	.99998	.99998	.99998	.99998	.99999	.99999	.99999

for $t > 3$ $\operatorname{erf}(t) \approx 1 - \frac{1}{\sqrt{\pi}\, t} \exp(-t^2)$

erfc (t) = 1 - erf (t)

End of Paper